REMARKS

Claims 1-8, 10, 12-27 and new claim 28 are pending in the application. Claim 9 has been cancelled by this amendment.

The applicants respectfully submit that no new matter has been added.

Claims 1-8, 10, 15 and 16 stand rejected under 35 USC §103(a) as being unpatentable over Shibasaki et al. (U.S. Patent No. 5,430,310) in view of Ishikawa (U.S. Patent No. 6,294,446).

In brief, Shibasaki's device is a low-noise high-frequency FET, which is much different from the now claimed high power device. Shibasaki uses words "high frequency" and "high gate breakdown voltage," but does not use the words "high power." As will be explained below, these expression have separate exclusive meanings. Shibasaki teaches improving "breakdown voltage" at a Schottky junction of a gate electrode, which is unrelated to the invention as now claimed. Furthermore the "simple structure" of Shibasaki and "a super-lattice buffer layer" of Ishikawa in fact teach away from each other and are not compatible with each other.

First, Fig. 2B and Fig. 23 of Shibasaki show a low power operation, about 10mA x 1.5V or 30mA x 1.5V at most. On the other hand, Fig. 5 of the present application shows a high power operation, about 3400mA x 16V. A break down voltage does not appear in Fig. 5 of the present application, and therefore the breakdown voltage of the present invention exceeds 16V, which is much higher than Shibasaki's breakdown voltage of 1.2 - 1.6V, which can be

understood from the description on lines 52 - 54, column 12 of Shibasaki.

Lines 55-56, column 16 of Shibasaki describes "best in high speed operation and noise characteristics." Therefore, Shibasaki's device is a low-noise high-frequency FET, which is much different from a high power device.

"A high gate breakdown voltage" appearing on lines 41-42, column 16 of Shibasaki means a minimum gate breakdown voltage for realizing a normal current-voltage characteristics at a Schottky junction, that is "a good rectifying characteristic."

Again "a high gate breakdown voltage" is not related to "a high power device."

Claim 1 has been amended to positively recite in the body of the claim, that a high power device is produced, i.e., "..communication formed therein, wherein said substrate, buffer layer and active layer, together form said high power semiconductor device."

Finally, Applicants emphasize that if Shibasaki were modified to include the super lattice buffer layer of Ishikawa, the modification ***would*** change the principal operation of Shibasaki because the Shibasaki's requirements for the buffer layer would not be met, which requirements Shibasaki teaches are critical for ensuring high electron mobility, thermal stability, low parasitic capacitance, ability to absorb the stress generated by lattice mismatch, etc.

Claim 9 stands rejected under 35 USC §103(a) as being unpatentable over Shibasaki et al. (U.S. Patent No. 5,430,310) in view of Ishikawa (U.S. Patent No. 6,294,446) and further in view of Usagawa et al. (U.S. Patent No. 5,373,191).

Claim 9 is dependent on claim 1 and therefore the rejection is addressed overcome based on the showing presented for the patentability of claim 1.

Claims 12-14 and 17-19 stand rejected under 35 USC §103(a) as being unpatentable over Shibasaki et al. (U.S. Patent No. 5,430,310) in view of Ishikawa (U.S. Patent No. 6,294,446) and further in view of Udagawa et al. (U.S. Patent No. 6,462,361).

Claims 12-14 and 17-19 are directly or indirectly dependent on claim 1. Accordingly, since the rejection over Shibasaki in view of Ishikawa has been addressed, this rejection will be moot.

With regard to the Examiner's comments as to functional language, set forth on page 5, second paragraph, of the Final Office Action, claims 17-19 have been amended order to recite the function in terms of the structure.

Claims 10, 20-22 and 24-27 stand rejected under 35 USC §103(a) as being unpatentable over Udagawa et al. (U.S. Patent No. 6,462,361).

The Examiner states that Udagawa discloses a compound GaAs substrate 301 having a resistivity of 3×10^7 Ohms-cm.

It is noted that all of the working examples of Udagawa teach a GaAs single crystal substrate having a total resistivity of less than 1.0×10^8, i.e., substrates 301, 601, 901, 111, and 121. See also independent claims 1-3, the abstract, col. 4, lines 63-64, col. 7, lines 63-64, col. 8, line 1, and lines 6-7, col. 13, lines 17-26, and col. 17, lines 55-67.

Udagawa does not to suggest a compound substrate, let alone a compound substrate having a total resistivity of more than1.0×10^8, as presently required.

The Examiner contends that it would have been obvious to the skilled artisan to form the compound semiconductor substrate having a resistivity of more that 1.0×10^8 Ohm-cm in total in order to reduce the resistance of the semiconductor substrate. The Examiner points to lines 52-54, col. 9 and Fig. 3 of Shibasaki, in support of his position.

The noted passage of Shibasaki states that "The term 'semi-insulating substrate' herein used means those having a resistivity of 10^7 Ohm-cm or higher." Shibasaki teaches that GaAs substrates are preferred because they provide high-quality semi-insulating single crystal substrates.

Udagawa requires a GaAs single-crystal substrate, and states that semi-insulating GaAs single-crystal substrates are preferred.

Present claim 10 requires a compound semiconductor substrate having a resistivity of less than 1.0×10^8 Ohm-cm at least at a surface thereof, and requires that the compound semiconductor substrate has a resistivity more than 1.0×10^8 Ohm-cm in total.

The skilled artisan in view of Udagawa and in view of the fact that semi-insulating GaAs single crystal substrates are those having a resistivity of 10^7 Ohm-cm or higher and in view of a desire to reduce resistance of the device, would not be motivated to modify Udagawa to produce the presently claimed high power semiconductor device comprising a compound substrate having two distinct resistivities.

Udagawa teaches a single-crystal, semi-insulating GaAs substrate, where "semi-insulating" means having a resistivity of 10^7 Ohm-cm or more as taught by Shibasaki. Udagawa teaches single-crystal, semi-insulating GaAs substrates having a resistivity of 2 or 3 x 10^7 Ohm-cm.

Nowhere does Udagawa or Shibasaki, suggest a compound substrate having a resistivity of less than 1.0 x 10^8 Ohm-cm at a surface thereof and more than 1.0 x 10^8 Ohm-cm in total, i.e., a compound substrate having two distinct resistivities, as presently required.

Claim 10 has been further amended to positively recite a "high power" semiconductor device.

Claim 23 is rejected under 35 USC §103(a) as being unpatentable over Udagawa et al. (U.S. Patent No. 6,462,361) in view of Shibasaki et al. (U.S. Patent No. 5,430,310).

Claim 23 is dependent on claim 10, and the rejection is addressed above.

In view of the aforementioned amendments and accompanying remarks, all claims are believed to be in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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